

CLAIM AMENDMENTS

1.-7. (Cancelled)

8. (Currently Amended) A method comprising:

amplifying data signals received from a memory bus, the memory bus comprising communication lines indicating the data signals and indicating at least one data strobe signal associated with a timing of the data signals;

sampling the amplified data signals; and

~~selectively enabling triggering enablement of the amplification in response to an edge of said at least one data strobe signal.~~

9. (Previously Presented) The method of claim 8, wherein the selectively enabling the amplification comprises:

selectively enabling sense amplifiers.

10. (Previously Presented) The method of claim 8, wherein the selectively enabling the amplification comprises:

selectively enabling the amplification in response to the beginning of the predetermined operation.

11. (Previously Presented) The method of claim 8, further comprising:

synchronizing the enabling of the amplification to the edge of said at least one data strobe signal.

12. (Previously Presented) The method of claim 8, further comprising:

communicating signals associated with a double data rate memory bus over the memory bus.

13. (Original) The method of claim 8, wherein the predetermined operation comprises a read operation.

14. (Original) The method of claim 8, wherein the predetermined operation comprises a write operation.

15.-20. (Cancelled)

21. (Currently Amended) An apparatus comprising:

amplifiers to amplify data signals received from a memory bus, the memory bus comprising communication lines indicating the data signals and indicating at least one data strobe signal associated with a timing of the data signals;

a first circuit coupled to the amplifiers to sample the amplified data signals; and  
a second circuit to selectively enable trigger enablement of the amplifiers in response to an edge of said at least one data strobe signal.

22. (Original) The apparatus of claim 21, wherein the second circuit selectively disables the amplifiers in response to the end of a particular read operation.

23. (Original) The apparatus of claim 21, wherein the predetermined operation comprises a read operation.

24. (Original) The apparatus of claim 21, wherein the predetermined operation comprises a write operation.

25. (Original) The apparatus of claim 21, wherein the apparatus comprises a memory controller.

26. (Original) The apparatus of claim 21, wherein the apparatus comprises a memory device.

27.-28. (Cancelled)

29. (Currently Amended) A computer system comprising:  
a memory;  
a memory bus coupled to the memory;  
a processor to initiate a predetermined operation with the memory over the memory bus, the memory bus comprising communication lines indicating the data signals and indicating at least one data strobe signal associated with a timing of the data signals;  
amplifiers to amplify data signals received from the memory bus;  
a first circuit coupled to the amplifiers to sample the amplified data signals; and  
a second circuit to ~~selectively enable~~ trigger enablement of the amplifiers in response to an edge of said at least one data strobe signal.

30. (Original) The computer system of claim 29, wherein the predetermined operation comprises one of a read operation and a write operation.

31.33. (Cancelled)

34. (Currently Amended) A method comprising:  
amplifying data signals received from a memory bus, the memory bus comprising communication lines indicating the data signals and indicating at least one data strobe signal associated with a timing of the data signals;  
sampling the amplified data signals; and  
~~enabling~~ triggering enablement of the amplification in response to an edge of said at least one data strobe signal.

35. (Previously Presented) The method of claim 34, wherein the enabling the amplification comprises:

selectively enabling sense amplifiers.

36. (Previously Presented) The method of claim 34, wherein the enabling the amplification comprises:

selectively enabling the amplification in response to the beginning of the predetermined operation.

37.-39. (Cancelled)

40. (Currently Amended) An apparatus comprising:

amplifiers to amplify data signals received from a memory bus, the memory bus comprising communication lines indicating the data signals and indicating at least one data strobe signal associated with a timing of the data signals;

a first circuit coupled to the amplifiers to sample the amplified data signals; and  
a second circuit to ~~enable~~ trigger enablement of the amplifiers ~~in response~~ to an edge of said at least one data strobe signal.

41. (Previously Presented) The apparatus of claim 40, wherein the predetermined operation comprises a read operation.

42. (Previously Presented) The apparatus of claim 21, wherein the predetermined operation comprises a write operation.